Microwave and mmW Switch Technologies

Timothy Boles
MACOM Technology Solutions
Lowell, Massachusetts 01851 USA
timothy.boles@macom.com

***Abstract*— All high frequency radio and radar applications require electronically controlled functional operation in the form of high performance switches. This control functionality often must satisfy a number of requirements, such as, linearity, high isolation, low distortion, minimal signal loss, high third order intercept, switching speed, and power handling; in addition to simply being able to switch RF signals from one electrical path to another. This paper compares the performance and the ability to adopt either of two alternate GaN HEMT technologies to incumbent PIN diode, GaAs pHEMT, and SOI CMOS technologies**

Keywords—GaN HEMT; PIN diode; GaAs pHEMT; SOI CMOS; super lattice FET; high powrer switches; RF switches; IL; ISO; IIP3

I. INTRODUCTION

All high frequency radio and radar applications require electronically controlled functional operation in the form of high performance switches. This control functionality often must satisfy a number of requirements, such as, linearity, high isolation, low distortion, minimal signal loss, high third order intercept, switching speed, and power handling; in addition to simply being able to switch RF signals from one electrical path to another. Historically, high frequency switching was accomplished utilizing chip and wire, hybrid assembled, discrete components, most typically silicon based PIN diodes.

As the frequency of operation for both communication and radar surveillance increased, including a demand for improved overall switch capability, integrated RF, microwave, and mmW frequency switches as monolithic components became a necessity. These monolithic control components have been produced using technologies as varied as silicon PIN diodes, silicon MOSFET's, GaAs PIN diodes, GaAs MESFET's, GaAs pHEMT's, and silicon/silicon-on-insulator PIN diodes and MOSFET's; have been available since the 1980's; and employed in numerous commercial and military applications. Initially, all of these approaches were capable of only simple functionality and were limited in terms of power handling to a few tens of milliwatts of RF energy.

As the state-of-the-art of RF monolithic switch development advanced, the design complexity increased from simple single pole-single throw, series configured, relatively narrow bandwidth structures to multiple pole-multiple throw, broadband, multiple series, multiple shunt, and multiple series-multiple shunt constructed switches. Over this same timeframe, the maximum incident RF power handling also increased into the range of 30 dBm to 33 dBm. Within the last few years, GaAs pHEMT, SOI MOSFET's, AlGaAs vertical PIN diode, and SOI PIN diode technologies and switch configurations have developed approaches to address many of the fundamental thermal limitations associated with the underlying basic material properties and have produced high frequency switches capable of handling incident power levels that range up to 10 watts to 100 watts of continuous wave RF energy.

Recently, microwave and mmW control components based upon GaN HEMT technologies utilizing silicon carbide, sapphire, or high resistivity silicon substrates are being proposed as an alternative to more traditional silicon and GaAs approaches. This paper will discuss the advantages and limitations of these GaN HEMT technologies for high power switch functions.

II. DISCUSSION

While it has taken over a decade of developmental effort at various universities and industry laboratories, Gallium Nitride HEMT transistors and MMICs have begun to supplant silicon and GaAs in commercial and military RF, microwave, and mmW power amplifier applications. The reasons for this is clear if the intrinsic properties of GaN are compared to the previous technologies. An examination of the critical parameters of breakdown electric field, 10x when contrasted to silicon or GaAs; dielectric constant, approximately 50% reduction when put side by side against silicon, GaAs, or SiC; and dramatically increased power density are judged against silicon or GaAs, GaN has a clear-cut advantage for high frequency, high power applications.

It would seem that a natural progression of GaN HEMT devices into the domain of high power control components, specifically high power, RF, microwave, and mmW switches, is straightforward. This is especially true if the incumbent high power, high frequency switch technology that is based upon PIN diode topologies, which add the complexity of requiring current control and the associated driver circuitry, is contrasted to a FET based approach which only requires voltage control to accomplish the switching function. However, this logical extension of GaN into the power switch arena has seriously lagged the adoption that has been observed in the power amplifier field.

The primary reason for this delay in adoption can be seen in Figure 1 and Figure 2, which are plots, respectively, of insertion loss and isolation as a function of frequency for a commercially available DC to 12 GHz, 20 watt, GaN HEMT based SPDT switch. While this GaN HEMT high voltage

device technology as applied to high frequency switch implementation is specified to handle 43dBm of RF incident energy, the insertion loss and isolation are visibly less than world class when compared to alternate device and material approaches. The insertion loss in X-Band is approximately 1.0 dB and degrades substantially when the frequency of operation is pushed into Ku-Band. Isolation on the other hand is at an acceptable level of 30 dB over the X-Band to Ku-Band transition range, but is certainly degrading as the frequency as the frequency approaches Ka-Band.

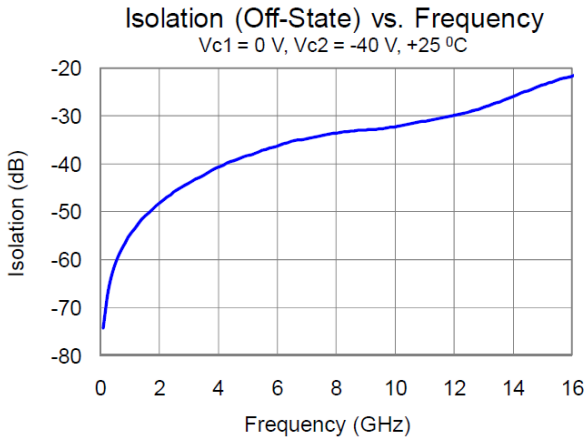

Fig. 1. Insertion Loss vs Frequency for Commercial, DC-12 GHz, High Power, GaN Switch

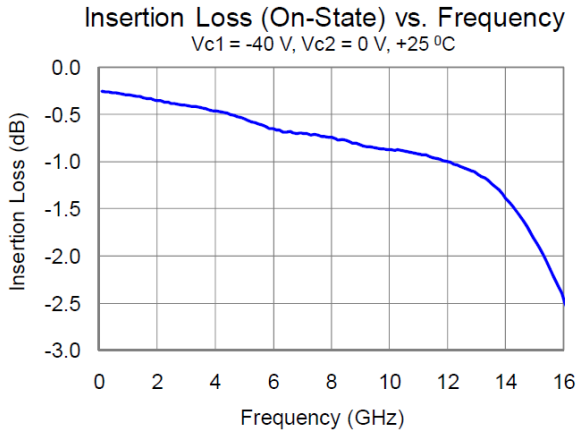

Fig. 2. Isolation vs Frequency for Commercial, DC-12 GHz, High Power, GaN Switch

The first issue can be seen in the IV response for a typical GaN HEMT shown in Figure 3. By observing the slope of the turn-on characteristic of the drain current vs drain voltage plot, it can be observed that the overall ON-resistance of a typical well performing HEMT structure is relatively high, on the order of several ohm*mm. The ON-resistance is simply the sum of sheet resistance of the 2DEG in the extended drain region necessary to support the high breakdown voltage, the intrinsic channel resistance, the ungated access resistance adjacent to the source and drain ohmic contacts, and the built-in ohmic contact resistance. An artifact of this high ON-resistance can also be seen in Figure 3 and is the fact that the typical GaN HEMT structure has a relatively high knee voltage, limiting the maximum RF swing during high frequency operation, and in turn, restricts the maximum power that is able to be transferred through the device.

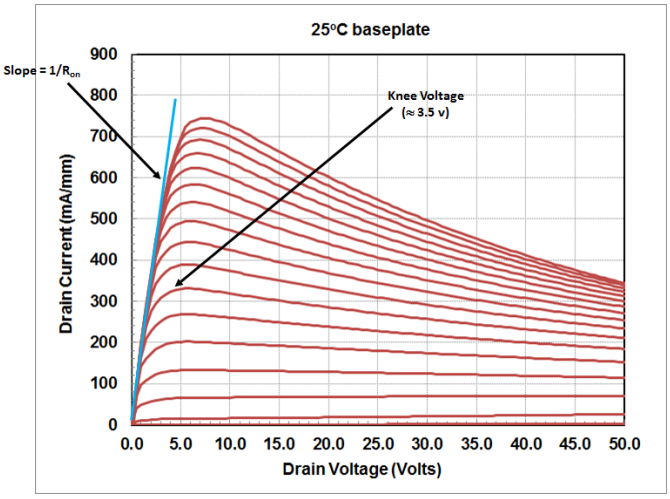

Fig. 3. Characteristic IV curves for a typical GaN HEMT

The effect of this relatively high ON-resistance on RF switch performance can be qualitatively examined by an analysis of the simplified impedances for series, shunt, and series/shunt switch configurations presented by a generic electrical device at microwave frequencies as presented in equations (1) through equation (6) below.

$$\text{Series } IL = 20 \cdot \log_{10}\left[1+\left(\frac{R_S}{2 \cdot Z_0}\right)\right] \quad (1)$$

$$\text{Series } ISO = 10 \cdot \log_{10}\left[1+\left(\frac{X_C}{2 \cdot Z_0}\right)^2\right] \quad (2)$$

$$\text{Shunt } IL = 10 \cdot \log_{10}\left[1+\left(\frac{Z_0}{2 \cdot X_C}\right)^2\right] \quad (3)$$

$$\text{Shunt } ISO = 20 \cdot \log_{10}\left[1+\left(\frac{Z_0}{2 \cdot R_S}\right)\right] \quad (4)$$

Series-Shunt

$$IL = 10 \cdot \log_{10}\left[\left(1+\frac{R_S}{2 \cdot Z_0}\right)^2+\left(\frac{Z_0+R_S}{2 \cdot X_C}\right)^2\right] \quad (5)$$

Series-Shunt

$$ISO = 10 \cdot \log_{10}\left[\left(1+\frac{Z_0}{2 \cdot R_S}\right)^2+\left(\frac{X_C}{2 \cdot Z_0}\right)^2 \cdot \left(1+\frac{Z_0}{R_S}\right)^2\right] \quad (6)$$

As presented in the above equations, the series ON-resistance, R_S/R_{on}, and the OFF-state capacitance, C_T/C_{OFF}, leads to basic equations for insertion loss (IL) and isolation (ISO) of each topology of switch, as given below, with the assumption that R_S/R_{on} and C_T/C_{OFF} of both series and shunt elements are identical. It should also be kept in mind that these are first-order approximations and do not include interconnect parasitics, nor the effect of adding multiple arms to the switch. In practical designs, these secondary effects

must be accounted for, and one can take advantage of ¼ wave transformations in the case of shunt diode designs and impedance matching in all cases.

Examing the effect of the ON-resistance characteristic of a typical active element, it can be demonstrated by equation (1) that for a series only configured switch, the insertion loss, IL, is dependent entirely on the value of the on-state series resistance and the off-state total output capacitance is essentially decoupled from the switch insertion loss. For a series/shunt configured switch, equation (5), while the output capacitance does play a role, examination of the simplified equation for this switch configuration reveals that it too is dominated by the device on-state series resistance. Another way of viewing this series resistance dependence for series configured switches, the RF energy in the "on" arm is flowing through the active element. It can be seen from the above equations that the insertion loss and in direct proportion the RF power handling is limited by the losses and dissipation in this series element.

A similar evaluation can be made for shunt configured switches, as shown in equation (3). In this case the RF energy in the "on" arm is not flowing through the active device, but instead is being transferred from input to output through low loss, high Q transmission lines. In this case the RF dissipation is primarily due to I^2R losses in the metallic conductors with the active blocking element being DC reverse biased in an off-state. The insertion loss in this shunt configuration, as expressed in equation (3), is limited only by the output shunt capacitance, and for multi-throw configurations the loss in the λ/4 wave transformers need to provide isolation between switch arms, and the IL will result in low values even for active device structures that have significant series on state resistance. The difficulty in this all shunt switch configuration, as can be seen in equation (4), is that a high ON-state resistance will result in degraded isolation, ISO. If the forward on resistance is too high the isolation in each switch arm may be so poor as to render the switch unusable.

In comparison, the ON-resistance of a typical GaAs pHEMT FET, as shown in Figure 4, is less than 1.0 ohm*mm with value of approximately 0.75 ohm*mm extracted from the

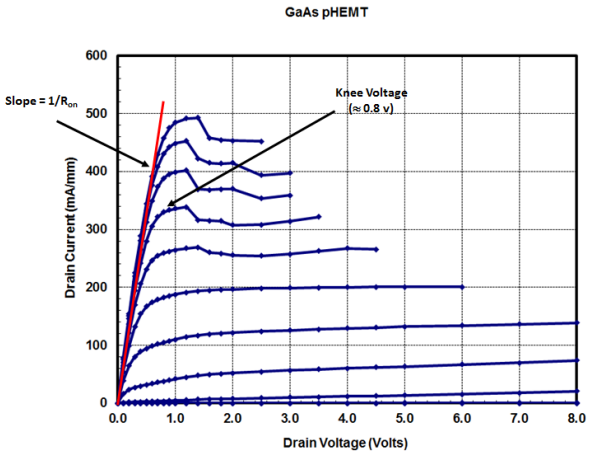

Fig. 4. Characteristic IV curves for a typical GaAs pHEMT

slope of the transfer curve. Combining this typical pHEMT ON-resistance with a characteristic OFF-capacitance of 300 fF/mm leads to a $R_{ON}C_{OFF}$ figure of merit of 224 fsec, which is very significant improvement over the high voltage

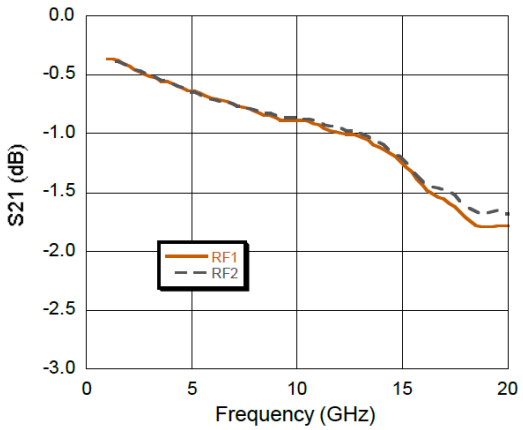

Fig. 5. Insertion Loss vs Frequency for a Commercial DC-20 GHz SPDT GaAs pHEMT Switch

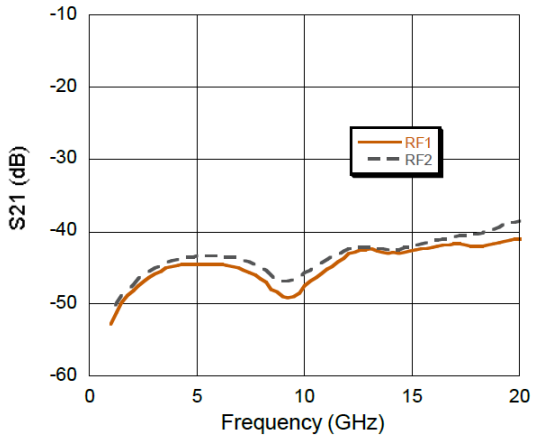

Fig. 6. Isolation vs Frequency for a Commercial DC-20 GHz SPDT GaAs pHEMT Switch

GaN HEMT structure. It can also be seen that the corresponding knee voltage is much lower with an approximate value of 0.8 volts, enabling larger RF swings during switch operation.

The effect of this lower knee voltage and ON-resistance on pHEMT RF switch performance can be seen in Figure 5 and Figure 6. Figure 5 is a plot of insertion loss from DC to 20 GHz for a 1.0 watt SPDT switch and is approximately 0.9 dB through 10 GHz and less than 1.8 dB at 20 GHz. Figure 6 is a similar frequency plot for isolation for the same SPDT switch and it can be observed than an excellent isolation of greater than 40 dB is obtained over the DC to 20 GHz range. While this insertion loss and isolation clearly outperform the GaN switch, it should be kept in mind that the input power handling of this GaAs pHEMT structure is only a few watts.

When CMOS based silicon SOI MOSFETs are considered as the active element for high power, high frequency switches, it is found in the literature that ON-resistances between

1.0 ohm*mm and 2.0 ohm*mm are readily achieved. In addition, OFF-capacitances of 250 fF/mm to 300 fF/mm for these high frequency MOSFETs are able to be realized simultaneously. These active component values lead to a $R_{ON}C_{OFF}$ figure of merit that approaches values observed on GaAs pHEMT switch device designs and results in overall switch performance is very competitive from RF through microwave frequencies.

This performance can be observed in Figure 7 and Figure 8, which are plots of insertion loss and isolation from

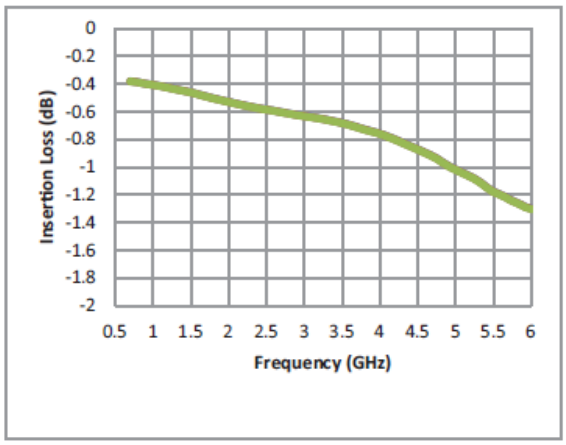

Fig. 7. Insertion Loss vs Frequency for a Commercial DC-6 GHz SPDT SOI MOSFET Switch

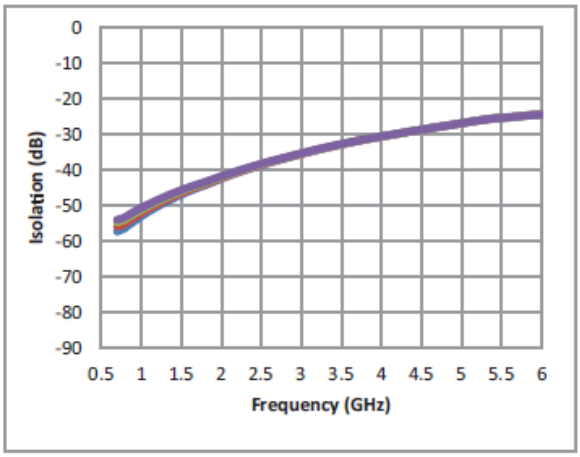

Fig. 8. Isolation vs Frequency for a Commercial DC-6 GHz SPDT SOI MOSFET Switch

DC to 6 GHz for an 8.0 watt SPDT switch. It can be seen that the insertion loss is between 0.4 dB and 0.8 dB from DC to 4.0 GHz and degrades 1.5 dB at 6 GHz. Correspondingly, isolation of greater than 30 dB is obtained over the DC to 4 GHz range, while again degradation in performance is observed as the frequency approaches 6.0 GHz.

For non-FET structures, i.e. PIN diodes, the corresponding limiting parameters are the series resistance in the ON-state, R_S, the OFF-state junction capacitance, C_T, and a corresponding figure of merit, the R_SC_T product.

The development of the heterojunction AlGaAs/GaAs PIN diode first reported application of a wide bandgap engineering being applied to create a heterojunction in place of a conventional p-n junction. This development was one of those rare improvements in a semiconductor device structure that only enhances the diode RF and microwave performance with no trade-off in any other characteristic.

Bandgap engineering principles were used to create a structure using two dissimilar semiconductor materials which have different Fermi levels to produce a device that has a wider bandgap in the P+ anode region as compared to the I-region. This difference in bandgap enables a suitable barrier height difference to be created, which both enhances forward injection of holes from the P+ anode into the I-region and retards the back injection of electrons from the I-region into the P+ anode under forward bias. This results in a PIN structure that has a significantly higher concentration of charge carriers reducing the RF resistance in the I-region of the heterojunction PIN device. The capacitance of the diode will remain unchanged since the thickness and resistivity of the I-region are unchanged. Measurements of fabricated diodes demonstrated an approximate 3 dB reduction of RF resistance in an appropriately formed AlGaAs/GaAs PIN diode vs. a GaAs homojunction PIN diode under forward bias. The RF capacitance of the same two diodes under reverse bias was identical, as expected.

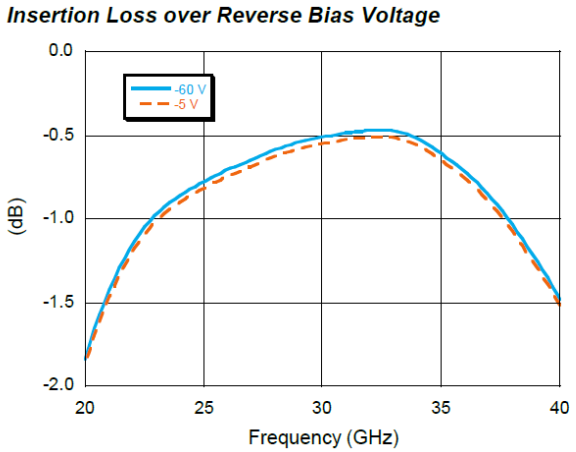

Fig. 9. Insertion Loss over Reverse Bias vs Frequency for a Commercial 40 watt, 24-37 GHz SPDT AlGaAs/GaAs PIN Diode Switch

A typical AlGaAs/GaAs heterojunction PIN diode when operated in a forward biased state has less than 5.0 ohms of RF series resistance. The reversed bias off-capacitance at 10.0 GHz for this same structure is typically 0.018 pF. These component parameter values lead to a R_SC_T figure of merit of approximately 94 fsec. When compared to the $R_{ON}C_{OFF}$ figure of merit reported by other FET technologies, this R_SC_T value is less than one third of the best reported FET/pHEMT devices.

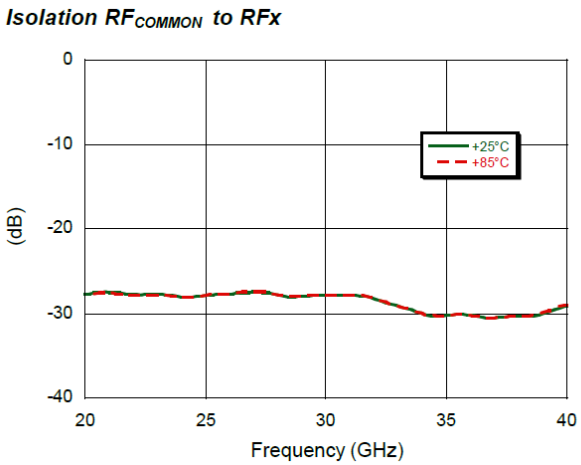

Fig. 10. Isolation over Temperature vs Frequency for a Commercial 40 watt, 24-37 GHz SPDT AlGaAs/GaAs PIN Diode Switch

Applying this basic building block to the shunt switch topology discussed above, a high power mmW SPDT switch capable of handling 40 watts of CW RF energy over a 24 GHz-37 GHz frequency range was developed. This high power handling performance was achieved while demonstrating <0.7 dB of insertion loss, >25dB isolation, as shown in Figure 9 and Figure 10, and >60 dBm IIP3. To the author's knowledge, this is the highest power handling available in any switch technology at mmW frequencies.

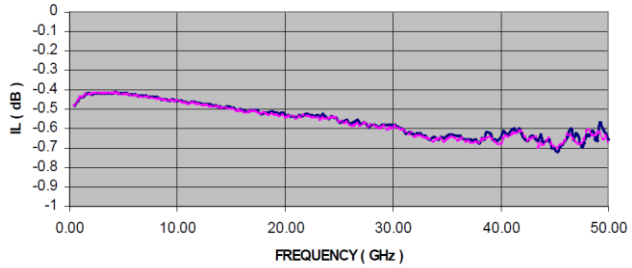

Fig. 11. Insertion Loss vs Frequency for a Commercial 50 MHz to 50 GHz SPDT AlGaAs/GaAs PIN Diode Switch

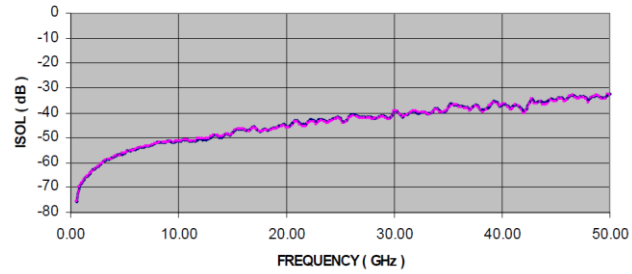

Fig. 12. Isolation vs Frequency for a Commercial 50 MHz to 50 GHz SPDT AlGaAs/GaAs PIN Diode Switch

In addition, when this fundamental device structure is utilized in a series-shunt broadband switch topology, multi-throw designs ranging from SPST through SP8T were able to be realized. These designs easily achieved broadband performance from 50 MHz to 70 GHz, with a typical insertion loss of 0.6 dB and isolation >30dB at 50 GHz, as shown in Figure 11 and Figure 12 for an SPDT broadband AlGaAs/GaAs PIN diode switch..

HMIC is a glass/silicon patented technology that enables silicon PIN diodes to be monolithically integrated into virtually any standard switch topology utilizing a borosilicate glass to provide all requisite DC and RF isolation between the active elements. As with the AlGaAs/GaAs PIN diodes, the basic silicon PIN diode building block have been characterized relative the fundamental RF series on resistance, the reverse bias off capacitance, and the R_SC_T product figure of merit.

In this HMIC/silicon PIN diode switch technology, the diode design has been optimized separately for series and shunt active elements. For the series PIN diode structure the forward biased on-state has less than 3.0 ohms of RF series resistance. The reversed bias off-capacitance at 1.0 GHz for this same structure is typically 0.030 pF. These component parameter values lead to a R_SC_T figure of merit of approximately 90 fsec. Similarly for the shunt PIN diode, it can be seen that the forward biased on-state RF resistance is roughly 1.9 ohms, with a reverse bias off-capacitance of approximately 0.10 pF, and a R_SC_T figure of merit about 190 fsec.

Applying these basic PIN diodes to the shunt switch topology discussed previously, high power SPDT T/R switches capable of handling 120 watts of CW RF energy at L-Band and 20 watts of CW RF power at X-Band have been produced. This high power handling performance was achieved while demonstrating <1.0 dB of insertion loss, >35dB isolation, Figure 13 and Figure 14, and >60 dBm of IIP3 at these microwave frequencies.

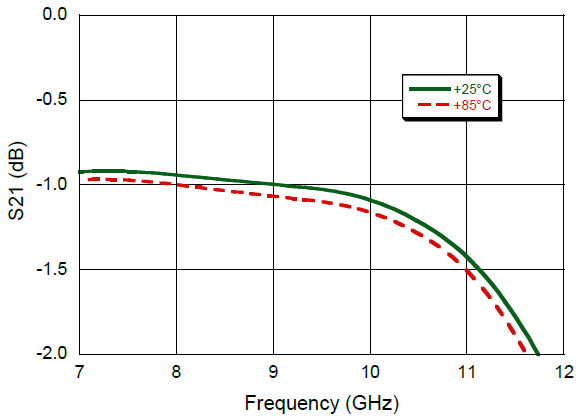

Fig. 13. Insertion Loss Over Temperature vs Frequency for a Commercial 20 watt, 8 GHz to 10.5 GHz SPDT HMIC PIN Diode Switch

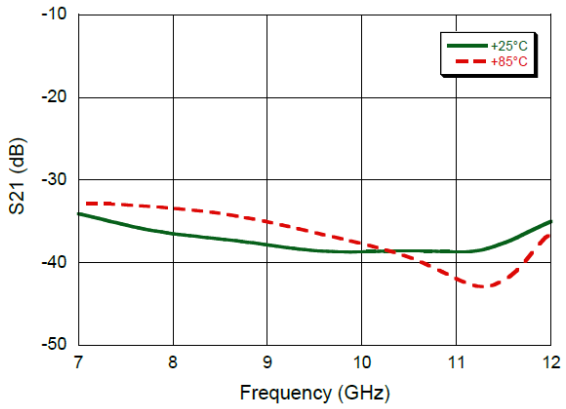

Fig. 14. Isolation Over Temperature vs Frequency for a Commercial 20 watt, 8 GHz to 10.5 GHz SPDT HMIC PIN Diode Switch

In addition, when these fundamental device structures are utilized in a series-shunt broadband switch topology, multi-throw designs ranging from SPST through SP6T were able to be achieved. These designs easily attained instantaneous broadband performance from 20 MHz to 26 GHz, with a typical insertion loss <0.9 dB, isolation >30dB, and 33 dBm of RF power handling at 26 GHz.

A comparison of key operational parameters of operational frequency range, insertion loss, isolation, input third order intercept, and CW power handling, that have been extracted from literature and industrial sources for typical SPDT switch topologies, for gallium nitride HEMT switches relative to AlGaAs and silicon based PIN diode; GaAs MESFET; and SOI CMOS switching control components is presented in Table I. It is easily seen in Table I that power handling capabilities GaN HEMT devices that have been readily demonstrated in power amplier design and development have carried over to GaN HEMT based high frequency switches. It is clear that GaN HEMT switch technology easily out performs more traditional switch technolgies relative to power handling except for AlGaAs and HMIC/silicon PIN diode integrated control functions. The difficulty with this GaN HEMT approach for switch applications is the relatively high insertion loss and low isolation compared to other switch technologies which is a direct result of the higher ON-resistance that is typically observed on GaN HEMT power transistors.

TABLE I
COMPARISON OF SWITCH OPERATIONAL PARAMETERS

Switch Technology	Frequency	IL	ISO	IIP3	CW Power Handling
	(GHz)	(dB)	(dB)	(dBm)	(watts)
GaN HEMT	DC-18	1.50	25	NS	20
GaAs pHEMT	DC-5	0.90	35	56	1
AlGaAs PIN Diode	0.01-70	0.60	48	60	40
HMIC/Silicon PIN Diode	0.01-30	0.20	45	72	120
SOI CMOS	DC-6	1.30	33	70	7
NS = Not Specified					

To be specific, it can be seen that the IL for a typical GaN HEMT is on the order of 1.5 dB for switch that is specified at a 20 watt CW power handling. This contrasts dramatically with AlGaAs PIN diodes switches which are capable of operating over a much broader frequency range, specified up an input CW power of 40 watts, and has a typical insertion loss of 0.4 dB. This difference in performance is more striking for raw power handling for HIMC/silicon based switches, where CW input power levels of up to 120 watts are routine with an IL of 0.2 dB.

A very interesting approach to high power GaN based switches that has been reported in the literature by both university and industrial investigators is a multi-channel super lattice HEMT structure. This technology fundamentally reduces the HEMT total ON-resistance and resultant knee voltage by utilizing super lattice MOCVD epitaxial growth techniques to layer alternating AlN and GaN layers resulting in a parallel stack of a number of 2DEG channels. This 2DEG configuration can be simply modeled as resistors in parallel resulting in the single FET channel resistance being divided by the number of super lattice periods. A typical AlN/GaN super lattice epitaxial structure is shown schematically in Figure 15.

The super lattice FET, (SL FET) is a three dimensional transisrtor structure. The SL FET is carved out of the basic

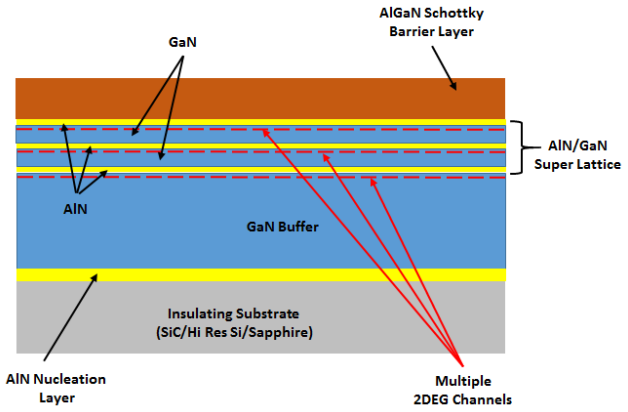

Fig. 15. Schematic crossection of a typical AlN/GaN super lattice epitaial structure with multiple 2DEG channels

epitaxil stack by depositing metallic source and drain ohmic contacts to the 2DEG layers. A two sided mesa is then formed by etching vias with tapered sidewalls perpendicular to the source and drain ohmic contacts. The SLFET is completed by depositing a metallic gate along the tapered via wall and contacts each supper lattice period contolling bias to the corresponding 2DEG. The three dimensional aspects of the SL FET and the unique source, drain and especially the gate contacting schemes are presented in Figure 16.

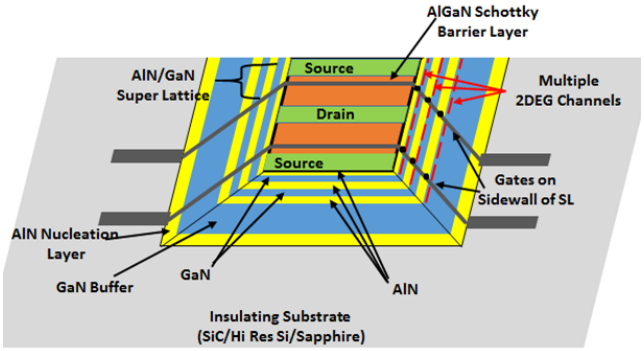

Fig. 16. Conceptual schematic of three dimensional SL FET

Virtually all of the university investigations that have been presented in the literature have generally concentrated on the specific aspects of the generation of the multiple channel super lattice structure. The publications from this quarter have included alternate III-V materials for the Schottky barrier layer, specific supper lattice dimensions, the probable effects on mobility and charge conentration in the multiple 2DEG channels, and possible source, drain, and gate contacting schemes.

The author has located only one published reference that not only discusses the aspects of the development of an AlGaN/GaN super lattice epitaxial structure but also has actually produced and characterized a high frequency RF and microwave switch. In this publication, the investigators chose an acronym of SLCFET, a "Super-Lattice Castellated Field Effect Transistor, in light of the unique three dimensional switch design and gate contacting configuration.

The RF performance results of this power switch developmental effort has been reproduced in part to complete the comparison to both RF switches based upon power amplifier GaN HEMT structures, and more traditional GaAs pHEMT, AlGaAs PIN diodes, HMIC/silicon PIN diodes, and SOI CMOS technologies. This data can be seen in Table II below.

TABLE II
COMPARISON OF SL FET SWITCH OPERATIONAL PARAMETERS

Switch Technology	Frequency	$R_{ON}C_{OFF}/R_SC_T$	IL	ISO	IIP3	CW Power Handling
	(GHz)	(fsec)	(dB)	(dB)	(dBm)	(watts)
SL FET	DC-18	136	0.60	30	62	4
GaN HEMT	DC-18	2500	1.50	25	NS	20
GaAs pHEMT	DC-5	224	0.90	35	56	1
AlGaAs PIN Diode	0.01-70	94	0.60	48	60	40
HMIC/Silicon PIN Diode	0.01-30	190	0.20	45	72	120
SOI CMOS	DC-6	485	1.30	33	70	7
NS = Not Specified						

In Table II, it can be seen that the SL FET/SLCFET concept has achieved a low insertion loss of 0.6 dB, a very respectable RF isolation of 30 dB, and high linearity with a third order intercept popint of 62 dBm. However, the present CW power handling of the super lattice FET switch of 4 watts is unimpressive and certainly requires additional developmental effort, but it would seem reasonable than a straightforward increase the total FET periphery would enable this FET switch structure to be able to achieve tens of watts of CW input power handling. Bottom line, the super lattice FET topology appears to be the only GaN technolgy that has the potential to deliver GaAs pHEMT/AlGaAs PIN diode/HMIC-Silicon PIN Diode switch performance with respect to range of frequency of operation, low insertion loss, high isolation, and high IIP3 linearity, and provide the desired, less complex, voltage only operation characteristic of a FET based technology.

III. CONCLUSION

While the use of GaN HEMT transistors for high frequency, high power switches is an apparent logical extension based upon the market accepted GaN high power discrete device and MMIC technologies as applied to amplifiers, but this has proved not to be the case. While the ability to handle tens of watts of CW incident power has clearly been demonstrated for GaN HEMT switch topologies, this power handling has come at the cost of reduced frequency of operation, high insertion loss, and poor RF isolation. This especially true when compared to current PIN diode, high power switch topologies and the resultant performance covering RF through mmW frequencies.

A new GaN technology, Based upon a AlGaN/AlN/GaN super lattice structure that is just now emerging from universities and R&D laboratories holds the best promise to achieve PIN diode IL, ISO, and IIP3 performance without the associated drawbacks of the requirement of current control and complex driver circuitry.

However, when a comparison is made across all the switch technologies at a fundamental level, by examining the $R_{ON}C_{OFF}/R_SC_T$ product for the basic active elements for each material technology in Table II, it can be seen that the AlGaAs/GaAs PIN diode topology is the distinct winner with a R_SC_T product of 94 fF while standard high power GaN HEMT structure is by far the poorest with a $R_{ON}C_{OFF}$ product of 2500 fF, which over a factor of 20x higher. Based upon these elementary device characteristics, the ONLY clear answer for a SPDT switch capable of high power handling, mmW operational frequencies, low insertion loss, high isolation, low distortion, and excellent linearity is the AlGaAs/GaAs heterojunction PIN diode technology platform

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